CLAIMS

Please **CANCEL** claims 19-21 as follows:

A status of the claims is provided below.

1. (Original) A method of manufacturing a semiconductor structure, comprising the steps of:

forming a p-type field-effect-transistor (pFET) channel and a n-type field-effect-transistor (nFET) channel in a substrate;

forming a pFET stack in the pFET channel and an nFET stack in the nFET channel;

providing a first layer of material at source/drain regions associated with the pFET stack, the first layer of material having a lattice constant different than a base lattice constant of the substrate to create a compressive state within the pFET channel; and

providing a second layer of material at the source/drain regions associated with the nFET stack, the second layer of material having a lattice constant different than the base lattice constant of the substrate to create a tensile state at the nFET channel.

2. (Original) The method of claim 1, wherein the first layer of material is SiGe having a content of Ge approximately greater than 0% in ratio to Si.

3. (Original) The method of claim 1, wherein the second layer of material is Si:C.

4. (Original) The method of claim 3, wherein the Si:C has a content of C of about 4% or less.

5. (Original) The method of claim 1, wherein the first layer of material is unrelaxed SiGe and the second of material is unrelaxed Si:C and is formed at a thickness of about between 10 to 100 nm.

6. (Original) The method of claim 1, wherein:

the first layer of material is formed by placing a mask over the nFET channel and etching

the regions of the pFET and selectively growing the first layer of material within the regions of the pFET channel; and

the second layer of material is formed by placing a mask over the pFET channel and etching regions of the nFET and selectively growing the second layer of material within the regions of the nFET channel.

7. (Original) The method of claim 6, further comprising the steps of:

providing a protection layer under the mask and over the pFET stack prior to the etching of the regions of the pFET stack and selectively growing the first layer of material; and

providing a protection layer under the mask and over the nFET stack prior to the etching of the regions of the pFET stack and selectively growing the second layer of material.

8. (Original) The method of claim 1, wherein the first layer of material and the second layer of material are grown to a thickness about 10 to 100 nm.

9. (Original) The method of claim 1, wherein the first layer of material and the second layer of material are embedded in the layer.

10. (Original) A method of manufacturing a semiconductor structure, comprising the steps of:

forming a p-type field-effect-transistor (pFET) channel and a n-type field-effect-transistor (nFET) channel in a substrate;

forming a pFET structure and an nFET structure on the substrate associated with the pFET channel and the nFET channel, respectively;

etching regions of the pFET structure and the nFET structure;

forming a first material with a lattice constant different than a base lattice constant of the substrate in the regions of the pFET structure to provide a compressive stress in the pFET channel;

forming a second material with a lattice constant different than the base lattice constant of the substrate in the regions of the nFET structure to provide a tensile stress in the nFET channel;

and

doping source and drain regions of the nFET and pFET structures.

11. (Original) The method of claim 10, wherein the first material is SiGe and the second material is Si:C.

12. (Original) The method of claim 11, wherein:

the first material creates a compressive stress within the pFET channel; and

the second material creates a tensile stress within the nFET channel.

13. (Original) The method of claim 10, wherein:

the first material is formed by placing a protective layer over the nFET structure and the pFET structure and growing the first material within source and drain regions of the pFET channel; and

the second material is formed by placing a protective layer over the pFET structure and source and drain regions of the pFET structure and the nFET structure and growing the first material within source and drain regions of the nFET channel.

14. (Original) The method of claim 10, wherein the first material and the second material are embedded in the insulation layer.

15. (Original) The method of claim 10, wherein the first material and the second material are raised above a surface of the insulation layer.

16. (Original) The method of claim 10, wherein the first material and the second material are at a thickness of about between 10 to 100 nm.

17. (Original) The method of claim 10, wherein the first material is unrelaxed SiGe.

18. (Original) The method of claim 10, further comprising the step of in situ doping the first

material with p-type doping and the second material with n-type doping to form the source and drain regions of the pFET and nFET, respectively.

19-21. (Canceled)